

IN THE SPECIFICATION

Please delete the text on page 1 after "III-NITRIDE LIGHT-EMITTING DEVICE WITH INCREASED LIGHT GENERATING CAPABILITY" and before "CROSS REFERENCE TO RELATED APPLICATION."

Please replace paragraph [0040] with the following paragraph.

A1

[0040] In the cross-sectional view shown in Figure 6b, the device includes an III nitride epitaxial heterostructure of n-type ~~and undoped~~ layers 11 and p-type layers 12, each in contact with an active region 13. The ~~III-nitride~~ n-type layers 11 may include one or more undoped layers and are optionally attached to a transparent superstrate 10. The superstrate 10 can be the growth substrate for deposition of the III nitride layers. In the plan view of the bottom of the LED die shown in Figure 6a, the large area of the device ($> 400 \times 400 \mu\text{m}^2$) requires n-electrode 22 "fingers" interposing the p-electrode metallization 20 to spread current uniformly throughout the device. Such an electrode configuration is required in large-area devices to provide a low series resistance (to overcome the low conductivity III nitride layers) and thus provide a high maximum drive current as specified in Equation 3. Thus, the interposed n-electrode configuration is required for large-area devices for maximizing total light generation capability. The device is inverted so that light may be taken out through the transparent superstrate 10 as well as the sidewalls and provides good extraction efficiency by using a highly reflective, thick p-electrode metallization 20. The reflectivity of the p-electrode is such that its absorption at the LED emission wavelength is less than 25% per pass, as described above. The electrode metallizations connect to submount electrodes 52 on a submount substrate 50 via interconnects 60. The interconnects make electrical connection between the LED and the submount while providing a thermal path for heat removal from the LED during operation. Although the illustrated embodiments refer to solder, the interconnects may be made of elemental metals, metal alloys, semiconductor-metal alloys, solders, thermally and electrically conductive pastes or compounds (e.g., epoxies), eutectic joints (e.g., Pd-In-Pd) between dissimilar metals between the LED die and submount, Au stud-bumps, or solder bumps.

Please replace paragraph [0041] with the following paragraph.

A2

[0041] The interconnects are attached to the LED and submount via conductive interfaces 41, 54. When solder is used as the interconnect, the conductive interfaces are wettable metals.

42

An application process initially determines the interconnect thickness and area. One applicable technique is a screen-printing process where paste is applied to select areas on the submount wafer or LED. Other techniques include electro-plating, lift-off, and reflow. For an embodiment using solder as the interconnect, the final interconnect thickness and area are determined by the solder volume as well as the ~~wettable metals~~ conductive interfaces 41 on the LED die and 54 on the submount. The solderable areas on the LED are defined through patterning of the wetting metals, or through vias in a patterned dielectric passivation layer 42 provided on the LED die. The dielectric passivation 42 layer acts as an electrical isolation layer between the p and n electrodes and is required since the ~~solder layers~~ conductive interfaces 41 extend across both p and n electrodes. The solderable areas on the submount are similarly defined by patterning the solderable metals 54. In an alternate embodiment, the wettable areas of the metallization 54 may be defined by a patterned dielectric layer. A second set of solderable metal layers 55 may be deposited on the back of the submount for attachment to the package. Optionally, a suitable solder can be deposited directly on the back of the submount. Because the thermal conductivity of any underfill material between the LED and submount is very low, e.g. $<2.0 \text{ W/mK}$, the junction-to-package thermal resistance is largely governed by the die/submount solder joint and the submount material and geometry. Assuming heat generation at the p-electrode metallization and one-dimensional flow and ignoring the thermal resistances of thin layers and the submount-package solder joint, the junction-to-package thermal resistance may be written as

Please replace the abstract with the attached abstract.